

Contents

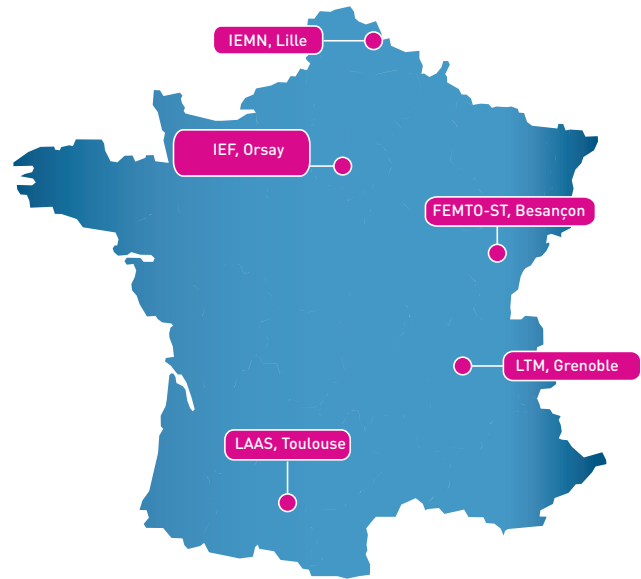
- Renatech information day
- Improved micro- and nano-structuring of titanium dioxide
- Inkjet printer ceraprinter x-series
- Vertical nanowire array based field effect transistors for ultimate scaling
- FEMTO-ST adds a new extension to its cleanroom
- Dual beam: fib and sem (equipment in LAAS)
- Ultra low noise HEMTS for deep cryogenic electronics
- III-V Cluster Launching

RENATECH information day 20th March, 2014, 10am – 4pm

The annual users' information day has become the traditional event for the academic and industrial micro- and nano-technological community. As in 2013 and 2012, this year manifestation will embrace the whole French territory and will be organized at the same day in all laboratories of large technological facilities. Thus participants will have an opportunity to know better the network facilities which are located in their areas and to visit the clean rooms. Close interactions with the local actors of the large technological facilities will provide an excellent opportunity to establish new contacts and to learn more about the procedures of project submission and its realisation in the network.

IEF and LPN facilities will welcome their users at IEF laboratory in Orsay, IEMN - in Villeneuve-d'Ascq, FEMTO-ST - in Besançon, LAAS - in Toulouse, LTM and CEA LETI - in Grenoble.

To participate at the users' information day, please confirm your participation directly at the technological facility of your choice.



Détecteur infrarouge hautes performances pour l'astronomie



Capteur autonome de pression et température réalisé en partenariat avec la société Schrader

Besançon(FEMTO-ST): mimento@femto-st.fr

Lille (IEMN): plateforme@iemn.univ-lille1.fr

Toulouse (LAAS): plateformertb@laas.fr

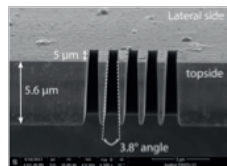
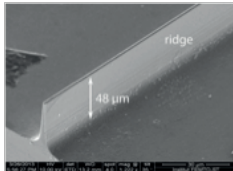
Grenoble (LTM/CEA LETI) cecile.gourgon@cea.fr ou thierry.billon@cea.fr

Marcoussis/Orsay (IEF) : centrale-techno@lpn.cnrs.fr ou ctu.ief@u-psud.fr

The development of nonlinear or electro-optical microresonators represents a stimulating challenge to achieve advanced functionalities in compact optical processing devices. An interesting approach consists of using high-reflectance Bragg gratings as building blocks for Fabry–Perot cavities. We have thus developed a set of techniques to etch giant aspect ratio nanostructures in lithium niobate. Actually, an 8 μm long Bragg grating on a Ti:LiNbO₃ ridge waveguide was fabricated by combining optical-grade dicing and focused ion beam milling [1]. The first step consists in fabricating a planar waveguide on X-cut wafer by titanium indiffusion. Then, in order to confine the modes laterally, a ridge structure is etched by optical grade dicing with a circular precision saw (DISCO DAD 3350). The prepared ridge is 5.6 μm wide at its top and 48 μm deep. This method allows us to simultaneously cut and polish the lateral sides of the ridge. The high confinement achieved is fundamental to enhance electro-optical and nonlinear effects in the waveguide. Finally, a Bragg grating with five air grooves is etched by FIB milling on the top of the ridge. This fabrication process offers the ability to etch indifferently from the topside or from the lateral side of the ridge. However, etching from the topside of the ridge inevitably leads to conical-shaped patterns in the depth of the ridge, with sidewall angle no better than 8° due to matter redeposition during

the etching process. This conical shape induces a major unwanted effect: transmitted and reflected light through the grating sinks into the substrate after a few periods only. However, if the pattern is milled from the lateral side of the ridge, the aspect ratio is just limited by the length of the lateral trenches. In the figure the grating shows a depth of 5 μm , but this depth can be easily increased by etching longer trenches along the sidewall. Now the trench sidewall angle is reduced from 8° to 3.8° as the FIB can go through the entire width of the ridge, which limits the matter redeposition during the etching. The Bragg grating was etched in less than 2 h with a probe current of 230 pA, a write field of 50 μm , a step size of 10 nm, and a dwell time of 0.1 ms.

This technological process gives the opportunity to fabricate gratings with quasi-parallel trenches together with giant aspect ratios improving its performance. In this device, the reflectivity reached 53% for TM polarization and 47% for TE polarization. We may note that the strategy used here for etching high aspect ratio nano- and micro-structures on LiNbO₃ can certainly be adapted on other hard to etch materials.



[1] Clément Guyot, Gwenn Ulliac, Jean Dahdah, Wentao Qiu, Maria-Pilar Bernal, Fadi Baida, and Nadège Courjal, "Optical characterization of ultra-short Bragg grating on lithium niobate ridge waveguide" OPTICS LETTERS, Vol. 39, No. 2 : 371--374 (Jan. 2014)

iemn Inkjet printer ceraprinter x-series

In 2012 IEMN purchased the CeraPrinter X-series inkjet deposition tool from Ceradrop. This device is the most accurate inkjet printer available on the market. It is dedicated to develop our activity in printed electronic and bio-MEMS technologies.

The printer is equipped with two multi-nozzles print heads (128 nozzles) and a single-nozzle jet micro-dispenser mounted on the print head carrier. This enables the jetting of three various material during a single fabrication process with a motion accuracy of +/- 1,5 μm .

A wide range of inks are to be printed. For example the single-nozzle print head is used for the located deposit of biopolymers and enzymes (enzyme detection, bio-MEMS field). The two multi-nozzles print heads are used for both printing conductive and dielectric inks to allow the creation of transmission lines or microelectronic devices.

The users of the Ceraprinter also take advantage from its embedded post-process and software package making possible the designing of patterns, their printing and even their post-process analysis. Indeed the device has embedded reflectometer for thickness measurement, automated jetting analysis software providing a report on ejection reliability and a multi-layer printing mode giving access to the 3D printing.

Contact :

Isabelle Roch-Jeune : isabelle.roch-jeune@iemn.univ-lille1.fr

Colin Mismar : colin.mismar@iemn.univ-lille1.fr



Fig1: Mobil chuck and print head carrier



Fig 3: Print heads



Fig 3: CPW 2mm*200 μm ground plane

Vertical nanowire array-based field effect transistors for ultimate scaling

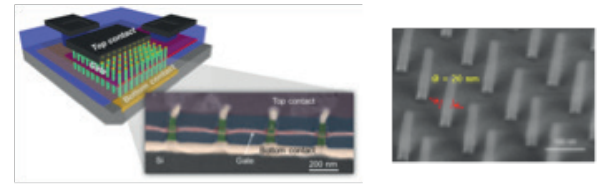
Nanowire-based field-effect transistors are among the most promising means of overcoming the limits of today's planar silicon electronic devices, in part because of their suitability for gate-all-around architectures, which provide perfect electrostatic control and facilitate further reductions in "ultimate" transistor size while maintaining low leakage currents. However, an architecture combining a scalable and reproducible structure with good electrical performance has yet to be demonstrated.

Here, we report a field-effect transistor implemented on dense vertical nanowire arrays with silicided source/drain contacts and scaled metallic gate length (14nm) fabricated using a simple process. The proposed architecture offers several advantages including better immunity to short channel effects, reduction of device-to-device variability, and nanometer gate length patterning without the need for high-resolution lithography.

In addition, these 3D transistors could be easily integrated into the conventional microelectronic devices used by the industry today.

The unique high-resolution lithography step is used for the NW patterning. In that framework, we achieved to perform high aspect ratio nanopillar array using low energy e-beam lithography. This work is based on the collaboration between LAAS-CNRS and IEMN.

Contact : Guilhem LARRIEU, glarrieu@laas.fr



Left: Nanopillar array patterning using low energy e-beam lithography. Right: Diagram of a 3D nano-transistor, and the related tilted view with transmission electron microscopy, showing the 14 nm gate (red) surrounding the vertical nanowires (green) and separating the contacts at the ends of each nanowire (beige).

FEMTO-ST adds a new extension to its cleanroom

In October 2013 we inaugurated a new extension to Mimento, the clean-room facility of FEMTO-ST, financed by the European Union (FEDER), the French government (CPER), the Franche-Comté Region and local institutions (Doubs department and Besançon community council). The extension has brought the total area of clean-room to 865m² of ISO 5, 6 and 7 zone. The reorganized space is now split between different areas corresponding to the different families of processes offered: photolithography (ISO 5 and 6), chemistry, thin-film deposition, plasma etching, nanotechnology, packaging (ISO 5) and characterization. Additionally, we provide space for biology and wet experiments, directly connected to the fabrication facilities. The clean-room is staffed by engineers for training of users, development of new processes and maintenance of equipment and facilities.

The engineers also work with research teams from FEMTO-ST and other labs and companies on cutting edge research projects.

A key evolution in this new configuration is that we tried to put in place a good environment for transfer between research and industry by making ample space for industry partners next to the space devoted to academic researchers. First, more than 25% of the area is devoted to an industrial line capable of small series production that is operated solely by staff from the startup company Frec'n'sys. This last constraint is imposed for ensuring high yield and repeatability as compared to the academic tools access based on multi-users operation. Additionally, there are 4 labs (about 15m² of ISO 7 space each) that can be rented out to companies for months or years to facilitate the development of prototype, perform clean assembly or packaging, etc. Finally, to foster even more this spirit, FEMTO-Engineering a private foundation for transferring to the industry the technologies developed at FEMTO-ST, will have some of its staff housed close to the facilities for stronger interaction with the engineers in charge of the equipment.



Dual Beam: FIB and SEM (Equipment in LAAS)

Operational date: June 2012

Helios NanoLab™ 600i, from FEI Company, is a system composed of two columns:

- a high resolution FEG-SEM (Field Effect Gun - Scanning Electron Microscope) : 0.9 nm at 15 kV
- and a FIB (Focused Ions Beam) column with Gallium source: 2.5 nm at 30 kV (using selective edge method)

It is completed by numerous accessories:

- 5 Gas Injection System (GIS) for:
 - Pt, Pd and SiO_x
 - Si and polymer etching accelerating gases
- Secondary electrons detectors: Inlens and outlens

- Backscattered electrons detector
- Secondary ions / Ion beam secondary electrons detector
- Transmitted electrons detector
- EDX: X-ray photons elementary analysis of materials

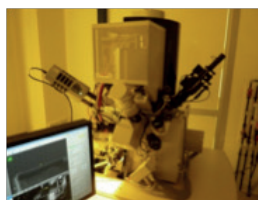
The Helios NanoLab™ 600i offers advanced ion and electron, imaging, patterning and deposition, as well as cross-sectioning, TEM lamella preparation and analysis down to the nanoscale. It is able to manage samples from few millimetres up to 6" wafers. The system can be fully automated using specific softwares for 3D tomography or electron/ion lithographies.

This equipment is a complete nano clean-room for prototyping!

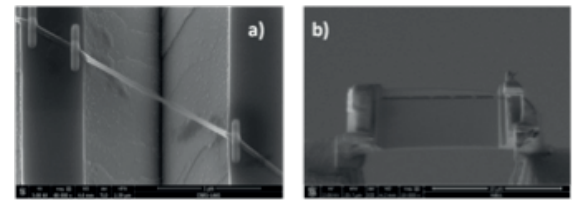
Contact:

Benjamin Reig, benjamin.reig@laas.fr

Franck Carcenac, franck.carcenac@laas.fr



The Helios NanoLab™ 600i installed in LAAS-CNRS



a) Creation of ankles on nanowire for AFM mechanical measurement, b) TEM Lamella



Ultra-low noise HEMTs for deep cryogenic electronics

To overcome the lack of high performance Field-Effect Transistors for high (and low) impedance, low-power and low-frequency deep cryogenic readout electronics, and to meet the needs of various experiments, from astrophysics to mesoscopic physics and low-temperature STM, a long-term investigation has been conducted at the CNRS/LPN. Thanks to the support, in part, from RENATECH network, significant progress was recently accomplished. LPN-fabricated cryogenic HEMTs now reach a better low-frequency noise level at $T \leq 4.2$ K than the record maintained since decades by the silicon JFETs from InterFET, which are limited to a temperature higher than 100 K. This achievement marks an important step for high performance cryoelectronics, and will lead to a better understanding of the $1/f$ noise in field-effect devices.

Application in mesoscopic physics:

The ultra-low voltage noise HEMTs are used to investigate quantum transport in mesoscopic circuits through extremely sensitive quantum shot-noise measurements. By implementing these HEMTs in a cryogenic amplifier at $T \leq 4.2$ K, together with a resonant circuit shifting the working frequency in the MHz range, we achieved an effective input voltage noise better than 0.25 nV/√Hz for measured samples of impedances as high as 100 kΩ.

Application for dark matter search:

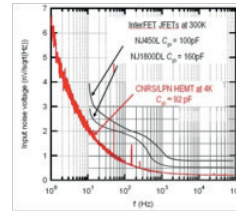
CNRS/LPN HEMTs at 4.2 K provide the unique possibility in terms of allowed power dissipation and noise performance for 100 Ge detectors (at 50 mK) readout electronics at 4.2 K. Compared to JFETs, by using CNRS/LPN HEMTs, first results show that the power consumption per transistor can be decreased by a factor of 70, and that the noise level can also be reduced.

Contact:

Y. Jin, yong.jin@lpn.cnrs.fr

Further reading: -The Role of the Gate Geometry for Cryogenic HEMTs: Towards an Input Voltage Noise Below 0.5 nV/√Hz at 1 kHz and 4.2 K, Q. Dong, Y. Liang, U. Gennser, A. Cavanna, Y. Jin, J. Low Temp. Phys. 167, 626 (2012)

-Input Noise Voltage Below 1 nV/√Hz^{1/2} at 1 kHz in the HEMTs at 4.2 K, Y. Liang, Q. Dong, U. Gennser, A. Cavanna, Y. Jin, J. Low Temp. Phys. 167, 632 (2012)



Noise characteristics comparison between the CNRS/LPN HEMT at 4.2 K and InterFET JFETs at 300 K.



CNRS/LPN HEMT in a ceramic package



III-V Cluster Launching

LTM-CNRS and CEA- Leti have jointly acquired a chemical vapor deposition epitaxy tool for the elaboration of III-V semiconductors on 300 mm silicon substrates. Deposition processes on these substrates will be studied in the framework of a joint development program (JDP) signed between CNRS, CEA and Applied Materials, the world's leading manufacturers of deposition tools in the field of microelectronics. In particular, compounds based on group III elements such as gallium, indium and aluminum and group V elements mainly arsenic and phosphorus will be explored. This equipment will be directly connected via a central platform, to a surface cleaning chamber and to a module allowing wafer transfer under vacuum directly to the epitaxy tool and other process or characterization modules. To be specific, the Equipex IMPACT project allows quasi in-situ physicochemical characterization of the epilayers by RAMAN spectroscopy, XPS, ellipsometry and photoluminescence. This is actually a unique tool that will analyze the impact of surface preparation and growth parameters on the physico-chemical properties of interfaces and epilayers grown on 300 mm Si substrates. Applications for these III-V layers on Si substrates include many areas like nanoelectronics, photonics, photovoltaics. This platform

will be accessible for laboratories and institutes through collaborative projects, via the RENATECH organization, which promotes networking in nanoelectronic and photonic areas.

Contact : thierry.baron@cea.fr



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To perform your project with RENATECH network

1. Register on www.renatech.org/projet/.
2. The application will be worked through and evaluated by the reception team.
3. Realize your project

For further information: renatech-accueil@cnrs-dir.fr

For further information concerning RENATECH Newsletter, please contact: caroline.boisard@cnrs-dir.fr

