RENATECH French national nanofabrication network

Newsletter

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Contents

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- Single-crystal thin films on 3 and 4-inch wafers by bonding and thinning techniques
- Probing the metal/ferroelectric interface electronic response to ferroelectric switching
- Combining low on-resistance with high breakdown voltage
- New equipment for 3D lithography
- Nitrogen doped Epitaxial Graphene on 4H-SiC(0001): Low Doping and High Charge transfer
- Collaboration between LTM/CNRS, CEA-Leti, Applied Materials and INLelectronics

RENATECH' Users meeting, on 20 th March, 2014

On the 20th of March, RENATECH users' meeting was held simultaneously in all the laboratories of the technological facilities. It was an excellent opportunity to inform the users about the latest technological competencies and equipment available in their regions, to overview the procedures of project submission and its realization as well as to visit the cleanrooms and to interact directly with the persons in charge of the technological facilities.

This year the meeting was organized in collaboration with the Enterprise Europe Network (EEN) managed by the Chamber of Commerce and Industry of each region (CCI).

The new web application form - https://www.RENATECH.org/ projet - has been demonstrated. A presentation from the CCI regarding regional funding concluded the morning session and from. NanoThinking, the French company of advice in nanotechnologies innovations, also presented his services. We gave the opportunity to exogenous project users (including SMEs and start-up) to present their experience in interacting with the RENATECH network. Finally, a visit of the clean-room was done during the afternoon session. A discussion with one visitor (a consulting company for innovation) for some more details on specific equipment for flexible electronics processing.

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Single-crystal thin films on 3 and 4-inch wafers by bonding and thinning techniques

The fabrication of single-crystal ferroelectric, piezoelectric, photorefractive, electro-optic, and nonlinear thin layers for radiofrequency, electro-acoustic and photonic integrated applications is an important technological challenge at FEMTO-ST Institute since several years. In this frame, home-made room-temperature bonding and wafer thinning techniques have been developed at MIMENTO so as to bond a large variety of different materials and to obtain micron-size, thickness-controlled, homogeneous thin layers while preserving the crystalline properties of the bulk materials. Two main wafer bonding techniques have been developed on 3 and 4-inch wafers. The first and most mature one is based on metal-metal adhesion, notably used for MEMS and RF applications (figure a). In this process, a gold laver is deposited on each wafer: the wafers are then bonded in a wafer-bonding equipment by applying a high pressure on the stack at room temperature. The second technique, mainly used for photonic applications, is based on glue adhesion (figure b). A UV-glue is deposited on the first wafer and then bonded onto the second one in the same waferbonding machine. The stack is then UV-exposed in order to polymerize the glue. In all cases the bondings are characterized by means of a homemade ultrasound bench, indicating that more of 98% of the achieved hybrid wafer interface is homogeneously

bonded. The single-crystal thin layer is then obtained by lapping and high-precision polishing techniques. On 3 and 4-inch wafers, the accuracy on the layer thickness is currently $\pm 1 \ \mu m$ and the surface roughness is inferior to 3 nm.

A representative ensemble of different bondings and different layer thicknesses is now mastered at MIMENTO and FEMTO-Engineering (figure c). The main bonded materials are silicon, quartz, lithium niobate, and lithium tantalate. The thinnest layer achieved on 3 and 4-inch wafers is 2 µm. More importantly, this technique allows keeping the crystalline properties of the original bulk materials while in a hybrid wafer format



Figures: Single-crystal thin films (a) SEM view of a lithium tantalate/gold/1.9um-thick lithium niobate stack, (b) SEM view of a silicon/UV-glue/7.5um-thick lithium niobate stack, (c) SEM view of a multiple layers stack with different materials.

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Probing the metal/ferroelectric interface electronic response to ferroelectric switching

The defining property of a ferroelectric (FE) material is a spontaneous macroscopic polarization which can be reversed under an applied electric field. Switching the polarization of such films requires a metallic contact, raising fundamental issues on the behavior of the interface between the FE layer and the electrode. Using X-ray Photoemission Spectroscopy (XPS) with in situ bias application, scientists from SPCSI (CEA / IRAMIS), Institut des Nanotechnologies de Lyon (INL) and Institut d'Electronique Fondamentale (IEF) have directly measured the band alignment and the electronic structure of ferroelectric BaTiO3 (BTO) near the Pt/BTO interface in a Pt/BTO/Nb-doped SrTiO3 (NSTO) heterostructure

IEF-Minerve (Figure 1a,b). Electrodes $300 \times 300 \ \mu m^2$ wide and 3 nm thick were patterned by ion beam etching. Thicker palladium pads overlapping part of the Pt electrodes were deposited to enable wire-bonding of the top electrodes to the sample holder. A highly insulating layer of Al2O3 was deposited onto bare BTO to suppress interference of the Pd pads with the capacitance (Figure 1a). At the TEMPO beamline of SOLEIL, the $100 \times 100 \ \mu\text{m}^2$ beam could be directed onto a single top electrode located by a map of the whole sample using the Pt absorption edge (Figure 1c).

The possibility to switch the FE polarization in situ allowed to put forward an experimental conduction-band offset depending on both the interface chemistry (Pt/BTO at the top and BTO/NSTO at the bottom) and the FE polarization [1]. Moreover, the timeresolved detection system available at TEMPO beamline was used to follow in operando the chemical/electronic changes in a ferroelectric capacitor [2].





The micro-fabrication of 20 identical Pt/BTO/NSTO capacitors

(300x300 µm²) on a 5x5 mm² surface was performed in the CTU

Figure 1: (a) Schematic of the capacitor; (b) Mask for optical lithography; (c) Pt 4f intensity map



Combining low on-resistance with high breakdown voltage



Institute of Electronic, Microelectronic and Nanotechnology (IEMN) in France and EpiGaN in Belgium have claimed a record combination of specific on-resistance and breakdown voltage for a double heterostructure field-effect transistor (DHFET) using a gallium nitride (GaN) channel and aluminum nitride (AIN) barrier on silicon (Si) substrate [Nicolas Herbecq et al, Appl. Phys. Express, vol7, p034103, 2014].

The backside processing involved thinning and polishing the Si substrate down to 230µm, followed by local deep reactive-ion etch to the AlGaN buffer layer using the 'Bosch process' on a Surface Technology Systems tool. The Bosch technique involves a sequence of passivation and etch steps, which results in reproducible vertical walls and allows high aspect ratios to be achieved. The local etch removed material around the drain contact (Fig.1).

The team tackled leakage problems from substrate conduction by locally removing silicon from beneath critical parts of the device to achieve a record combination of breakdown voltage (1.9 kV) with a specific on-resistance of 1.6 m Ω -cm2 (Fig.2).

The researchers believe that the technique could be used to extend the gate-drain spacing to ~30 μ m, allowing 3kV blocking to be reached with less than 5m Ω -cm2 specific on-resistance. Gate insulation would reduce leakage further. The team also suggests that a thick dielectric trench fill with, for example, AIN, could reduce self-heating effects.



Piezo Stage: 300 x 300 x 300 µm3 Motorized Stage: 100 x 100 mm2

Laser: 780 nm, < 120 fs, 80 MHz, > 120 mW

Microscope and Autofocus: objective 100 x, NA=1.30, WD=370 μm

Sample holder: 30 mm diameter

Application fields of this technology are very large. 3D lithography has been employed so far for 3D cell culture, 3D microfluidics, 3D photonics to name just few

of them. At LAAS-CNRS, this tool will be used in particular for the fabrication of 3D microcatheters to be inserted in vivo for the detection of rare circulating cancer biomarkers. By its design and appropriate simulations, the 3D microsystem will ensure the physical trapping of the desired species while preserving blood's native laminar flow. We will use biocompatible polymers for the fabrication of the structure and will explore its biochemical functionalization.

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Nitrogen doped Epitaxial Graphene on 4H-SiC(0001): Low Doping and High Charge transfer



Figure 1: (a) High-resolution N 1s spectra of

the nitrogen-doped graphene at h = 480 eV

(surface sensitive, top panel) and N 1s at h

= 600 eV (bulk sensitive, bottom panel). (b)

four suggested doping sites, i.e., graphitic, pyrrolic, and pyridinic nitrogen, and Si-N formation (side and top view). (c) Different configurations of N-doped graphene layer.

Sketch of nitrogen-doped graphene with the

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 Nitrogen doping of graphene is of great interest for both fundamental research to explore the effect of dopants on a 2D electrical conductor and applications such as lithium storage, composites, and nanoelectronic devices.

The electronic properties of epitaxial graphene are modified thanks to the introduction, during the growth, of nitrogen-atom substitution in the carbon

honeycomb lattice. High-resolution transmission microscopy and low energy electron microscopy investigations indicate that the nitrogen-doped graphene is uniform at large scale. The substitution of nitrogen atoms in the graphene planes was confirmed using high resolution X-ray photoelectron spectroscopy, which reveals several atomic configurations for the nitrogen atoms: graphitic-like, pyridine-like, and pyrrolic-like (figure 1). Angle-resolved photoemission measurements show that the N-doped graphene exhibits large n-type carrier concentrations of 2.6 1013 cm-2, about 4 times more than what is found for pristine graphene, grown under similar pressure conditions.

These experiments demonstrate that a small amount of dopants (<1%) can significantly tune the electronic properties of graphene by shifting the Dirac cone about 0.3 eV toward higher binding energies with respect to the band of pristine graphene, which is a key feature for envisioning applications in nanoelectronics.

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LAAS New equipment for 3D lithography

triggered by ultra-short laser pulses. The absorbed energy causes a chemical and / or physical change of the photoresist within a small volume pixel ("voxel"), which may be scaled by the laser power.

Therefore, the laser lithography system is used for the fabrication of specific structures by exposing the photosensitive material along trajectories and / or points defined by the appropriate designed 3D model. During the writing process, the position of the laser focus is controlled with nanometer precision using a piezo stage. Its main characteristics are the following: LTM/CNRS has worked altogether with CEA-Leti, Applied Materials and INL on ways to improve material quality for indium gallium arsenide compound semiconductors quantum wells grown on silicon substrates. The final objective is to incorporate III-V high mobility materials on silicon and thus boost transistor performances. One of the main problems with growing InGaAs and related materials on silicon is lattice mismatch, with differences of 4% for pure GaAs and 11% for InAs, compared with silicon, and difference in polarity induced anti phase domains (APD).

We have used "aspect ratio trapping" method, where the compounds semiconductor material was grown in trenches in silicon dioxide on 300 mm Si(100) substrates in an Applied Materials metal organic chemical vapor deposition system. The trenches were aligned in the [110] direction. A GaAs



FIBSTEM cross section of InGaAs/AIGaAs QW (R. Cipro, PhD)



SIMS profile of InGaAs/ AlGaAs QW (V. Gorbenko PhD)



pletely annihilate the APBs.

RT µPL signal in function of In in the QWs

with indium content. The FWHMs of the signals were around 60 meV.

nucleation layer was grown directly on the exposed silicon

surface at low temperature, followed by higher tempera-

ture growth (less than 550°C) of GaAs/AlAs/ InGaAs/AlAs/

GaAs. With just 180 nm GaAs grown in the trenches, the APB

density was found to decrease with the trenches width. An aspect ratio of 1.3 is demonstrated to be sufficient to com-

Scanning electron micrographs of GaAs in 1.3 aspect ratio

cavities suggest that misfit dislocations beginning at the Si/

GaAs interface were almost completely blocked by the SiO2

sidewalls. On this good quality GaAs buffer layers, AIAs/

InGaAs/AlAs/GaAs multilayers were grown inside the cavi-

ties. Samples with low AR trenches (<1.3) exhibit room tem-

perature µ-photoluminescence. The QWs emissions varied

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EVENTS MNE 2014 – 22th to 26th September 2014 in Lausanne at EPFL



MNE (Micro and Nano Engineering) is a major annual international conference, devoted to micro and nano engineering, held in a European country every September. The conference brings together engineers and scientists from across the world to discuss recent progress and future trends in the fabrication, manufacturing, operation and application of micro and nano-structures and devices. Applications in electronics, magnetics, photonics, electromechanics, environment and life sciences are also discussed.

As usual, RENATECH will participate to this event. You will find us at the booth 40

9th micro&nano brokerage event – 25th & 26th September 2014 in Besançon - France Micronora



+ enterprise europe network

Specifically designed to allow European actors to meet and discuss during pre-arranged B2B meetings, the brokerage events has been organized since 1998 and aims at foresting technical cooperation. Targeted mostly at companies, technical institution and research laboratories willing to promote their innovations or find solutions to develop new products, integrate new functionalities, improve existing technology....

Topics:

Advanced materials, smart materials, micro and nanomaterials, precision technologies (micromechatronics, micro and nanomanufacturing process), Micro and nano components design and products.

FEMTO-ST will participate at the brokerage event.

To perform your project with RENATECH network

- 1. Register on www.renatech.org/projet/.
- 2. The application will be worked through and evaluated by the reception team.
- 3. Realize your project

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