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### RENATECH : an integrated partnership of large nanotechnological facilities



RENATECH – the French national nanofabrication network– exists to facilitate all aspects of nanotechnology research by providing access to advanced nanotechnology instrumentation, processes and training. These recourses are provided through a supportive network of 6 leading academic nanotechnology laboratories supported by the French National Center for Scientific Research (CNRS) and the partner universities.

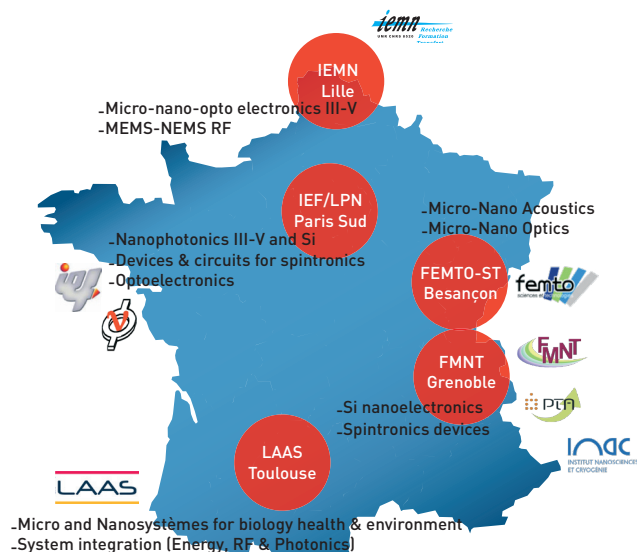
Central to the operation of RENATECH is the commitment to provide access to advanced technology for the entire nanotechnology community. With the rapid growth and unlimited potential of nanotechnology, it is critical that the scientific community enjoys appropriate accessible research resources. RENATECH facilities are open to the national and international scientific community and aim to provide diverse research projects with the best possible research conditions through an access to the high technology equipment and the staff expertise. To meet the challenge of providing broad access to state-of-the art technologies, RENATECH has highly developed education and training activities.

In order to assure that the network remains dynamic in its support and capabilities and makes judicious use of resources, RENATECH sites have defined technical focus areas. These areas correspond to the areas of major strength of the local research.

RENATECH facilities provide both geographical and technological diversity. Users are free to use any of the network sites or even

multiple sites. The external project applications, their descriptions and technological aspects are worked through and evaluated by reception team at each facility. The project analysis permits to define the process plan, to estimate its feasibility, costs and time schedule. If a facility is unable to realise the project for technical reasons, it will be referred to a more appropriate facility.

RENATECH is coordinated by the CNRS Institute for Engineering and Systems Sciences (INSIS) and is supported by the French National Research Agency (ANR) in the frames of the programme “National network of large technological facilities for Basic Technological Research”.





## Specific technological tools



### HF vapour etching for dry release of MEMS device at FEMTO-ST

The release step, used to free part of a micro device, is one of the most crucial process step. Actually, by using standard wet release there is both a high risk of catastrophic adhesion (stiction) during water rinsing and a strong possibility of breaking the device while drying with nitrogen. HF vapour has the advantage to etch easily inorganic materials, like silicon dioxide, but in a vapour phase thus without stiction. Thus, it is the technique of choice for SOI technology or surface micromachining, providing dry release of structures with no damage and no contamination. This etching is easy to carry out and requires only one step.

Moreover, contrary to HF wet etching, the vapour phase allows using several metals like aluminium, gold, platinum, etc as stop material or etching masks.

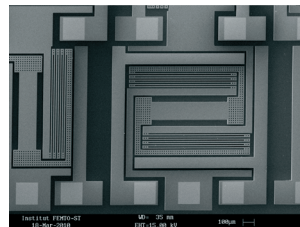
MIMENTO has acquired a new equipment of HF vapour phase etching from Idonus In the reaction chamber, the HF is liquid and diluted at 50% with water. The wafer chuck, which forms the lid,

is heated (between 35°C and 60°C) in order to control the vapour forming during the reaction and also the etch rate.

The 4 inch wafers are clamped mechanically with a clamping ring while clamping is electrostatic for smaller samples.

This technique has been used to successfully replace wet release and increase fabrication yield for an electrostatically actuated valve fabricated on SOI wafer. This valve is used for the control of air jet in a distributed actuator array for the ANR project Smart Surface.

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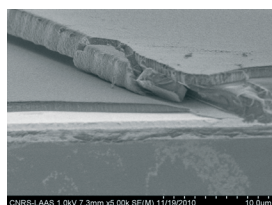


Electrostatic micro-actuator for air flow distributed micromanipulation

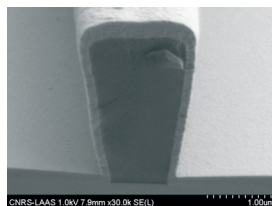


### PECVD LT (Plasma Enhanced Chemical Vapor Deposition at Low Temperature) Equipment at LAAS

Forecast operational date: February 2011



Step coverage of 50%



Step coverage of 0%

Everybody knows standard PECVD system for SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, a-Si deposition in which the decomposition of the reactive gases is obtained with capacitive coupled plasma on substrates heated at 300°C on average. The last plasma sources development give now the possibility to obtain very high species density using the induced coupled plasma technology able for instance to manage high current at high frequency.

Consequently, those progresses applied to such deposition equipment allow us, now, to deposit at very low temperature as ambient temperature, compare to 300°C, with correct dielectric properties of the materials. This is an important advantage to develop the "Electronic at Low Temperature" on polymers for example. Another advantage of such technique is to be able to do located deposition by using the Lift Off technique, process actually underdevelopment.

The problematic is here to control the step coverage of the deposition on photoresist lines as showed on the two following photographs. It is not also because we can do deposition at low temperature that we cannot also use high temperature.

So, in our equipment from OXFORD Company, deposition at 400°C is also possible. We plan to use such kind of deposition processes for optical applications for instance, research field well known for asking high thickness layers obtained with high deposition rate as the one that offers such PECVD reactor.

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## • New equipment corner :



### CO<sub>2</sub> Critical point dryer at PTA Toussimis Automegasamdri 815B-C

Or how to dry without destruction  
or avoid sticking of fragile structures



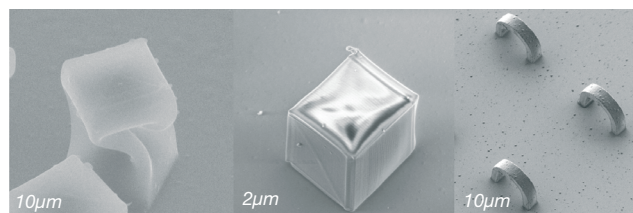
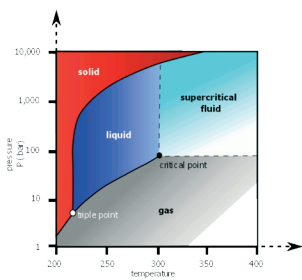
During evaporation internal structures that support the micro-object from inside are subjected to great surface tension forces resulting from density differentials, which occur when a liquid crosses the phase boundary into the gas phase during evaporation at atmospheric conditions.

Liquid CO<sub>2</sub> has two advantages: a low Critical Point at 74 Bar and 31°C and it is miscible with Alcohol.

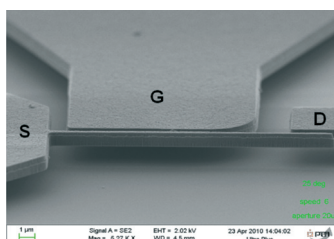
This facilitates our process to easily cross the Liquid/ Gas phase boundary with equal densities eliminating destructive surface tension forces.

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Drying of a 3D microstructures, obtained by polymerisation of resist by 2 photon laser absorption. The objects keep their shape because of their external surface only. The twisted cube has dried in normal air. The cube keeps its shape in the CO<sub>2</sub> CP Dryer; Michel Bouriau UJF LIPhy - UJF/CNRS



This Switch (Nano Electro Mechanical System) has been realized at the University of Stanford and the release of the device has been performed at the PTA and was characterized at IMEP-LAHC.

R. Hinchet et al, "Electrical and Mechanical Characterization of NEMS switches". Accepted to DTIP 2011- oral

presentation (International Conference on Design, Test, Integration & Packaging of MEMS/MOEMS), May 2011.



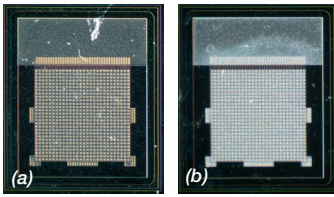
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## Recent technological realizations

LAAS

### Realization of a current and voltage bidirectional IGBT at LAAS



Front side (a) and backside (b) microphotograph of the realized bidirectional IGBT

The objective of this work carried out within the framework of MOBIDIC project (ANR-funded) and led by the LAAS in collaboration with the GE2Lab and CIME (Grenoble), and LMP (Tours) is to realize a bi-directional IGBT monolithically integrated in Si using two techniques: the first is based on the double-side photolithography and the second is based on Si/Si wafer bonding. This device is intended for AC/AC power converters requiring bi-directional switches. Compared to the currently used switches, the monolithic bidirectional IGBT makes it possible to reduce the number of components required to obtain the desired functionality and also to reduce the switching losses through an adequate control strategy. Our team has carried-out the realization as well as the characterization of bidirectional IGBT using the double-side photolithography. Moreover, we have developed on one hand a wafer thinning technological process that takes into consideration the Si/Si wafer bonding constraints and on the other hand a high temperature Si/Si wafer bonding step. The developed wafer thinning process allows to reduce the thickness of the silicon wafers with the perspective of carrying

a Si/Si wafer bonding in order to realize a bidirectional power semiconductor device. The Si wafer thinning step allows to optimize the thickness of the lightly doped region resulting from bonding and therefore reducing on-state losses. Our process allows today to thin functional silicon wafers down to 200  $\mu\text{m}$  thick. The resulting interface of Si/Si bonding must be mechanically robust and electrically transparent. Indeed, it must not lead to an increase in the on-state losses. This Si/Si wafer bonding step is fully integrated within the flexible IGBT process flow developed at LAAS and dedicated for the realization of power silicon semiconductor devices. Indeed, this bonding step makes use of the already existing high temperature N+ diffusion annealing step in order to consolidate the bonding. This annealing N+ diffusion step is required for the materialization of the N+ emitter region of the IGBT. Unlike low temperature bonding, very high temperatures (1050 °C) bonding allows a voids free interface. This process is validated by PIN diodes realizations. The next step concerns the validation of the bonding process on realizations of bidirectional IGBT.

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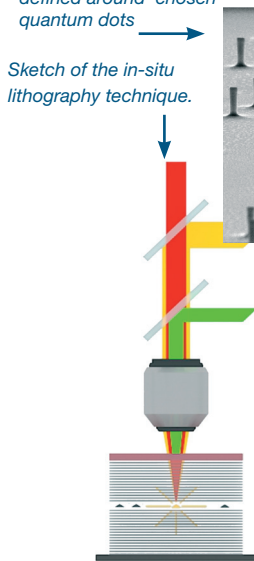
Abdelhakim Bourennane ([abourenn@laas.fr](mailto:abourenn@laas.fr))



### Optical lithography aligned on a nano-emitter at LPN

Field of micropillars defined around chosen quantum dots

Sketch of the in-situ lithography technique.



Nano-emitters such as quantum dots, colloidal quantum dots, fluorescent molecules, nanowires...are often randomly distributed on the surface of a substrate and suffer from broad inhomogeneous distributions of their spectral lines. As a result, the fabrication of devices based on single nano-emitters of known position and spectral characteristics is a technological challenge. The LPN has recently developed an in-situ lithography technique which allows defining a pattern around a selected nano-emitter. The sample embedding the single emitters is spin-coated with a positive photoresist. A first laser in the red spectral range is used to excite the emitter emission. By moving the emitter with piezo-actuators within the excitation spot and maximizing its emission intensity, one can determine the emitter position with 50 nm accuracy. A second laser (532 nm) is then used to expose the resist to define a pattern centred on the emitter. This whole procedure can be done at cryogenic temperatures (4K – 70 K). This technique has first been used to define micropillar cavities around semiconductor quantum dots. More recently, the same technique was used to insert a semiconductor quantum dot in a photonic molecule (coupled micropillars) so as to fabricate an ultrabright source of entangled photon pairs.

The technique was first implemented on a regular micro-photoluminescence setup. Recently, the LPN has developed a new machine to propose an in-situ lithography service. The machine was built by the Attocube society. This new setup allows an absolute positioning accuracy around 1 nm over a 1.2 mm x 1.2 mm sample region. The writing laser beam presents beam waist around 500 nm. Automatic scanning images can be done with the excitation laser to identify the emitter positions. The pattern writing procedure can then automatically be done with respect to these emitter positions. The setup has been delivered at LPN at the end of December 2010. We are currently adapting the resist exposure process to these new experimental conditions.



New in-situ lithography machine recently implemented at LPN

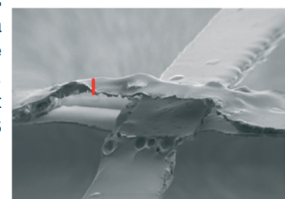
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### IEMN: Micromachining SU-8 pivot structures using AZ photoresist as direct sacrificial layers for a large wing displacement

A new processing method was proposed using AZ 4562 as sacrificial layers to create a controlled air-gap in the pivot region. This three-dimensional SU-8 pivot structures is designed to obtain a large wing displacement of the bio-mimetic flying micromachine. Several sacrificial methods used for the fabrication of SU-8 structures were reviewed and compared. A new process featuring AZ 4562 sacrificial layers was developed. For our process, the optimal pre-bake temperature of the AZ resist was found to be around 95 °C, which is consistent with the SU-8 bake temperature. Two relevant effects, the scission and out-gassing effects, were greatly weakened to acquire a better SU-8/AZ interface. It was found that AZ 4562 can be directly deposited on SU-8 without any barrier layer between AZ 4562 and SU-8. So, AZ 4562 can be used directly as a thick sacrificial layer, thus greatly simplifying the fabrication process. SU-8 reinforcing

patches can be added to compensate for the loss in thickness of the central beam in the pivot regions. Using this new method, SU-8 pivot structures with different central beams, either straight or L-shaped, was successfully materialized. The air-gap obtained is large and reaches ~100  $\mu\text{m}$ , thus helping to produce a large wing displacement. The fabrication precision and its main factors were evaluated. The deviation of actual structure size from design value was 2-7%, depending on the material and technique involved. Preliminary measurements of the fabricated structure show a large wing displacement, flexure angle and torsion angle can be achieved. This new process is simple, low cost and compatible with standard MEMS technology.



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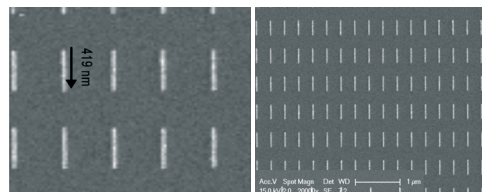




## Fabrication of infrared metamaterials for photonic applications at IEF

This work is part of the METAPHONIQUE project supported by the ANR funding agency. The main goal of this collaboration between IEF, LPN, UTT and Thales is to develop innovative photonic components based on metamaterials, i.e. artificial composites with optical properties that are not readily found in nature. The metamaterial shown here has been fabricated in the IEF clean room and consists of an array of Au nanowires on glass. The wire dimensions are much smaller than the wavelength of operation ( $\approx 1.55 \mu\text{m}$ ); their optical response has been carefully engineered so that the whole structure acts as an effective homogeneous medium with plasma-like properties. The fabrication process starts with coating the substrate with a negative PMMA resist in which the patterns are created by electron beam lithography. After developing the resist, the patterns are transferred to the glass substrate by Au evaporation and lift-off. A difficulty arises during the lithographic step because charges accumulate in the glass substrate while the sample is being exposed, result-

ing in uncontrolled features and structures of poor quality. To suppress this effect, a flash deposition of Ti was directly applied on the glass surface prior to resist coating. More work is now under way to fabricate multilayered samples in which interactions between nanowires of neighboring layers yield an artificial medium with a negative index of refraction. This new step represents a considerable technological challenge because the sample properties critically depend on the alignment between the different layers.



SEM micrographs of an infrared Au metamaterial with plasma-like properties. The length and width of the wires are about 420nm and 30 nm, respectively.

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## Events

### RENATECH users' information day

**Monday 21 march 2011, at the CNRS headquarters in Paris, Auditorium Marie Curie**

One of the main objectives of this event is to raise awareness of the national top-level infrastructure that provides the open, interdisciplinary, hands-on environment for scientists and engineers that enables them to use the advanced instruments of nanotechnology to bring their ideas to fruition.

RENATECH information day is the opportunity to learn about the main research thematic developed in the network, the principal technological means and competencies, as well as the procedures of project submission and its realisation in the network.

If you are interested, please follow the link for the registration: <http://projects.laas.fr/renatech>

Or confirm your participation to Elena Hoffert: [Elena.Hoffert@cnrs-dir.fr](mailto:Elena.Hoffert@cnrs-dir.fr)



## Realize your project with RENATECH network

1.Contact RENATECH network via:

common entrance point: [renatech-accueil@cnrs-dir.fr](mailto:renatech-accueil@cnrs-dir.fr)

or contact directly one of RENATECH facilities to discuss your application:



IEMN technological facility:

Contact: [plateforme@iemn.univ-lille1.fr](mailto:plateforme@iemn.univ-lille1.fr)



FEMTO-ST technological facility:

Contact: [mimento@femto-st.fr](mailto:mimento@femto-st.fr)



IEF technological facility:

Contact: [ctu@ief.u-psud.fr](mailto:ctu@ief.u-psud.fr)



LAAS technological facility

Contact: [plateformertb@laas.fr](mailto:plateformertb@laas.fr)



LPN technological facility

Contact: [centrale-techno@lpn.cnrs.fr](mailto:centrale-techno@lpn.cnrs.fr)



PTA technological facility:

Contact: [accueil@pta-grenoble.com](mailto:accueil@pta-grenoble.com)



2.The application will be worked through and evaluated by the reception team at each facility.

3.Realize your project

For further information concerning RENATECH newsletter contact: [Elena.Hoffert@cnrs-dir.fr](mailto:Elena.Hoffert@cnrs-dir.fr)



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